Organic monolayer dielectric for high-performance carbon nanotube transistors

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An ultrathin organic self-assembled monolayer gate dielectric is utilized to improve the performance of carbon nanotube transistors and to enable transistor fabrication on a wide range of substrates.

During the past years, single-walled carbon nanotubes (SWCNTs) have emerged as highly promising components of nanoscale devices. In particular, field effect transistors (FETs) based on semiconducting SWCNTs have attracted strong interest due to their excellent device characteristics.\(^1\)\(^,\)\(^2\) Such devices are usually implemented using a conventional three-electrode configuration comprising source (S) and drain (D) electrodes contacting the semiconductor (called channel, in our case the SWCNT, marked by a white arrow in Figure 1), plus a gate (G) electrode that is electrically insulated from source and drain by the gate dielectric (Figure 1). By applying a voltage to the gate electrode, the electrostatic potential in the channel and thereby its conductivity can be tuned.\(^3\)

In maximizing the performance of a transistor based on SWCNTs, the contacts made to the SWCNT channel, the integrity of the SWCNT itself, as well as the gate dielectric are of utmost importance. Three major requirements for a high-performance gate dielectric are: 1) High capacitance, which allows for transistor operation at low gate voltages, 2) good insulator properties to avoid undesirable gate leakage currents and 3) compatibility with a wide range of substrates.

In the most widely used configuration for SWCNT FETs, a highly doped silicon substrate covered with thermally grown silicon dioxide (SiO\(_2\); typical thickness 100-200 nm; growth temperature > 700 °C) serves as a macroscopic back-gate.\(^4\)

In our study we focus on the optimization of the gate dielectric. In order to obtain SWCNT-FETs with improved performance, we explored devices incorporating an organic gate dielectric comprised of a 2 nm thick self-assembled monolayer (SAM) formed on a Si/SiO\(_2\) substrate (4 nm thick SiO\(_2\) grown by plasma oxidation at room temperature), with the silicon substrate serving as back gate (Figure 1).\(^5\) The SAM is formed at a temperature of 200 °C and predominantly accounts for the excellent insulating properties of the dielectric stack: It reduces the leakage current by more than three orders of magnitude from 10\(^{-4}\) A/cm\(^2\) (4 nm SiO\(_2\) only) to 10\(^{-7}\) A/cm\(^2\). For a thin (6 nm), low-temperature processed, large-area dielectric this value represents an exceptionally small current density. Owing to their low formation
temperature, SAM gate dielectrics are compatible with unconventional substrates such as metallized plastic foils, thus enabling electronics on flexible substrates.\(^6\)

SWCNT-FETs with a channel length of 200 nm and AuPd contacts were fabricated via e-beam lithography. The transistors exhibit an unprecedented combination of excellent performance parameters. The output characteristic resembles that of conventional p-type semiconductor FETs, including saturation of the drain current at higher \(V_{ds}\) (Figure 2a). From the transfer characteristic of the devices (an exemplary one is shown in Figure 2b), a maximum transconductance \(g_m = \frac{dI_d}{dV_{gs}}\) of about 20 \(\mu S\) is determined at \(V_{ds} = -1\) V. This value is among the highest so far reported for SWCNT-FETs. In addition, the large ON/OFF drain current ratio of about \(10^5\) is remarkable in view of the small thickness of the gate dielectric and theoretical predictions on drain voltage scaling in SWCNT-FETs.\(^7\) Moreover, evaluation of the subthreshold swing \(S = \frac{dV_{gs}}{d(\log I_d)}\) yields a value of 60 mV/decade, which is very close to the theoretical limit at room temperature.\(^8\) Such a low value has not been previously reported for non-doped SWCNT-FETs with low operating voltages, and its realization within the present devices is notable considering that no attempts were made to reduce the contact resistance and that a global back gate is utilized.

![Figure 2](image)

Figure 2 (A) Output and (B) transfer characteristic of a SWCNT transistor comprising a self-assembled monolayer (SAM) based gate dielectric.

The transfer characteristics of SWCNT-FETs commonly display a hysteresis in the drain current.\(^8\) There have been a few reports of SWCNT-FETs where the hysteresis was reduced or eliminated by employing a liquid gate or by protecting the nanotube from air using inorganic dielectrics. In contrast, some of the SAM-based SWCNT-FETs presented in our work exhibit essentially no hysteresis despite the fact that a solid (i.e., more convenient) gate is employed and despite the fact that the CNT channel is exposed to air (Figure 2b). The lack of significant hysteresis in our SWCNT-FETs can be attributed to the hydrophobic nature of the SAM-modified dielectric surface which is expected to reduce the amount of adsorbed water. Surface water is well documented to enhance hysteretic behavior in nanotube FETs.\(^8\)

The strong gate coupling achieved in the SWCNT-FETs through integration of an ultrathin organic SAM as a high-quality gate dielectric with a low gate leakage current provides a highly versatile basis for further development of the transistors.